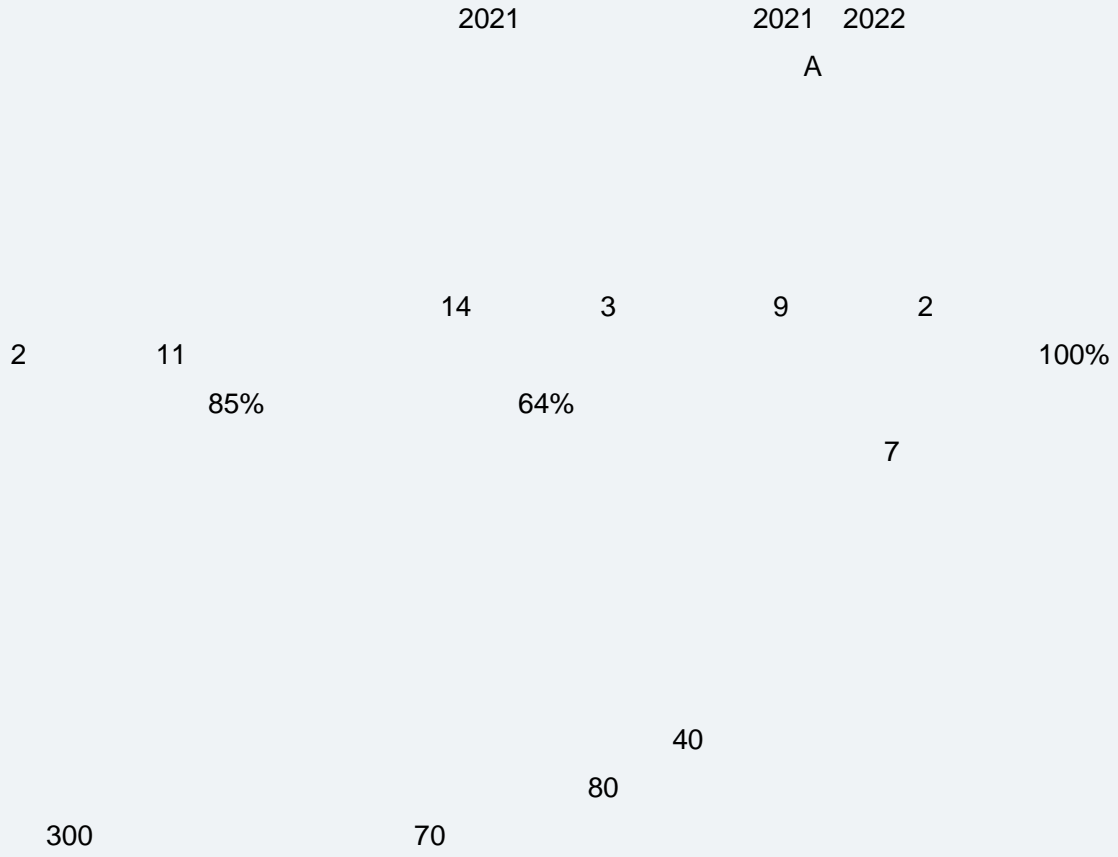


人工智能专业 2023 级人才培养方案

一、专业简介



二、培养目标

3

4

5

三、毕业要求

1

2

3 /

/

4

5

6

7

8

9

10

11

12

四、OBE 矩阵图

1

	1	2	3	4	5
1					
2					

		M
1.4		H
	AI	H
		H
		H
		M
		M
2.1		H
		H
		H
		H
		M
2.2		H
		H
	Python	H
		M
		M
2.3		H
		H
		H
		M

H

2.4

	3.3		H
			M
			H
			H
			H
			H
			H
			M
4	4.1		H
			H
			H
			M
			M
	4.2	Python	H
		FPGA	H
			H
			H
			M
	4.3		H
			H
			H
			H
			M
	4.4		H
			H
			H
		M	
		M	
5	5.1 Python) (C	I	H
		Python	H
			H
			M
			M
	5.2		H
		FPGA	H

			H
			H
			M
	5.3		H
		FPGA	H
			H
			M
			M
6.1		H	

			H
			H
			M
	8.2:		H
			H
			H
			H
			M
			M
			M
	9.1:		H
			H
			H
			M
			M
	9.2		H
			H
			H
			H
			M
			M
	10.1:	B	H
			H
			H
			H
		Python	M
	10.2:		H
		AI	H
			H
			M
	11.1		
			H

	11.2		M
			H
			H
			H
			H
			M
12	12.1		H
			H
			M
			M
			M
			M
	12.2		H
		(H
			H

H M L

五、专业特色/实践特色

AI

AI

六、学分要求

172.0

:

144.0	121.0	31.0
		28.0
		62.0
	23.0	14.0
		9.0
16.0		
12.0		

七、学制学位

4

八、指导性教学计划表

2023

COMA3G1001		3	48	16	3	1			
FLGA4G1001		3	48		3	1			
FLGA4G1002		3	48		3	2			
FLGA4G2001		3	48		3	3			
FLGA4G2002		3	48		3	4			
MARA2G1001		2	32		2	1			
MARA2G2002		2	32		2	3			
MARA3G1001		3	48		3	2			
MARA3G1002		3	48		3	1			
MARA3G2001		3	48		3	4			
PAEA1G1001		1	32	22	2	2			
PAEA1G2001		1	32	22	2	3			
PAEA1G2002		1	32	22	2	4			
		31.0							
								1.	
								2	
								2	
								" "	
								1	
CIE1V1E001		1	16			6			
CIE1V1E001		1	16			6			
CIE1V1E001		1	16			7			
		9.0							

ENGA2B1001	B	2	32		2	1		
MATA3B2001		3	48		3	3		
MATA3B2002		3	48		3	4		
MATA4B1001		4	64		4	2		
MATA6B1001		6	96		6	1		
PHYA2B1L01		2	32	32	2	3		
PHYA4B1001		4	64		4	2		
PHYA4B2001		4	64		4	3		
		28.0						
080702A4C2002		4	64	8	4	4		
080706C3C2004		3	48	12	3	5		
080717A3C2001		3	48	16	3	3		
080717A4C2008		4	64	16	4	3		
080717A5C1007		5	80	16	5	2		
080717C3C2002		3	48	16	3	4		
080717C3C2004		3	48	12	3	4		
080717C3C3005		3	48	16	3	5		
080717C4C2003		4	64	32	4	3		
080717E3C3006		3	48	16	3	5		
		35.0 (35.0 0.0)						
080717E2S2001		2	32	10	2	4		
080717E2S3002		2	32	16	2	5		
080717E2S3005		2	32	8	2	6		
080717E3S2006	FPGA	3	48	16	3	4		
080717E3S3003		3	48	16	3	6		
080717E3S3004		3	48	12	3	5		
080717E3S3007		3	48	24	3	6		
080717E3S3008		3	48	20	3	6		

		21.0 (21.0 0.0)						
080706C3S3002		3	48	12	3	5		
080706F3D3025		3	48		3	6		
080717C3D1001	AI	3	48	40	3	2		
080717C3D1002	Python	3	48	16	3	2		
080717D3D2007		3	48	16	3	4		
080717D3D3008		3	48	12	3	5		
080717F2D3003		2	32	10	2	5		
080717F2D3004		2	32	16	2	6		
080717F2D3005		2	32	14	2	6		
080717F2D3010		2	32	24	10	5		
080717F2D3011		2	32	8	2	6		
080717F2D4011		2	32	10	2	7		
080717F2D4012		2	32	10	2	7		
080717F2D4013		2	32	16	2	7		
080717F3D2006		3	48	16	3	3		
080717F3D3009		3	48	16	3	5		
		20.0 (6.0 14.0)						
080201COP1002	B	0.5	1()	1()		2		
080201COP3007		0.5	1()	1()		5		
080717COP2001		0.5	1()	1()		3		
080717COP3002		0.5	1()	1()		5		
080717C2P4007		2	4()	4()		7		
080717C3P4006		3	48	48		7		
080717EOP3003		0.5	1()	1()		6		
080717EOP4005		0.5	1()	1()		7		
080717E1P3004		1	2()	2()		6		
080717E7P4008		7	14()	14()		8		
		16.0 (16.0 0.0)						

MARA2Q1001		2	2()	2()	2	7		
MARA2Q4001		2	64			7		
PAEA1Q1001		1	32	32		1		
RAEA0Q1001		0.5	16			2		
RAEA0Q3002		0.5	16			5		
STUA0Q1001		0.5	16			1		()
STUA0Q1002		0.5	16			1		()
STUA1Q3001		1	32	24		6		()
STUA2Q1001		2	36			1		
STUA2Q1002		2	2()	2		1		()
		12.0 (12.0 0.0)						

1								
COMA3G1001		3	48	16	3			
ENGA2B1001	B	2	32		2			
FLGA4G1001		3	48		3			
MARA2G1001		2	32		2			
MARA3G1002		3	48		3			
MATA6B1001		6	96		6			
PAEA1Q1001		1	32	32	2			
STUA0Q1001		0.5	16					()
STUA0Q1002		0.5	16					()
STUA2Q1001		2	36	32	2			
STUA2Q1002		2	2()	2()				()
		25.0 0.0 ()						
2								
080201COP1002	B	0.5	1()	1()				
080717A5C1007		5	80	16	5			
080717C3D1001	AI	3	48	40	3			

080717C3D1002	Python	3	48	16	3			
FLGA4G1002		3	48		3			
MARA3G1001		3	48		3			
MATA4B1001		4	64		4			
PAEA1G1001		1	32	22	2			
PHYA4B1001		4	64		4			
RAEA001001		0.5	16		1			
		27.0		1.0		()		
3								
080717A3C2001		3	48	16	3			
080717A4C2008		4	64	16	4			
080717C0P2001		0.5	1()	1()				
080717C4C2003		4	64	32	4			
080717F3D2006		3	48	16	3			
FLGA4G2001		3	48		3			
MARA2G2002		2	32		2			
MATA3B2001		3	48		3			
PAEA1G2001		1	32	22	2			
PHYA2B1L01		2	32	32	2			
PHYA4B2001		4	64		4			
		26.5		3.0		()		
4								
080702A4C2002		4	64	8	4			
080717C3C2002		3	48	16	3			
080717C3C2004		3	48	12	3			
080717D3D2007		3	48	16	3			
080717E2S2001		2	32	10	2			
080717E3S2006	FPGA	3	48	16	3			
FLGA4G2002		3	48		3			
MARA3G2001		3	48		3			
MATA3B2002		3	48		3			

PAEA1G2002		1	32	22	2			
		25.0			3.0 ()			
5								
080201C0P3007		0.5	1()	1()				
080706C3C2004		3	48	12	3			
080706C3S3002		3	48	12	3			
080717C0P3002		0.5	1()	1()				
080717C3C3005		3	48	16	3			
080717D3D3008		3	48	12	2			
080717E2S3002		2	32	16	2			
080717E3C3006		3	48	16	3			
080717E3S3004		3	48	12	3			
080717F2D3003		2	32	10	2			
080717F2D3010		2	32	24	2			
080717F3D3009		3	48	16	3			
RAEA003002		0.5	16					
		15.5			10.0 ()			
6								
080706F3D3025		3	48		3			
080717E0P3003		0.5	1()	1()				
080717E1P3004		1	2()	2()				
080717E2S3005		2	32	8	2			
080717E3S3003		3	48	16	3			
080717E3S3007		3	48	24	3			
080717E3S3008		3	48	20	3			
080717F2D3004		2	32	16	2			
080717F2D3005		2	32	14	2			
080717F2D3011		2	32	8	2			
STUA103001		1	32	24	1			()
		13.5			6.0 ()			
7								

080717C2P4007		2	4()	4()				
080717C3P4006		3	48	48				
080717E0P4005		0.5	1()	1()				
080717F2D4011		2	32	10	2			
080717F2D4012		2	32	10	2			
080717F2D4013		2	32	16	2			
MARA2Q1001		2	2()	2()	2			
MARA2Q4001		2	64					
		9.5		0.0		()		
8								
080717E7P4008		7	14()	14()				
		7.0		0.0		()		